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Reg. No. : .....

Name : .....

Eighth Semester B.Tech. Degree Examination, April 2015
(2008 Scheme)
08.802 : COMPUTER SYSTEM ARCHITECTURE (R)

Time : 3 Hours Max. Marks : 100

PART – A

Answer **all** questions.

1. What is PRAM model ? Compare the different PRAM models.
2. List out the metrics affecting the scalability of a computer system for a given application.
3. Distinguish between register-to-register and memory-to-memory architecture for building conventional multivector supercomputers.
4. Explain how instruction set and memory hierarchy affect the CPU performance in terms of clock rate, program length and effective CPI.
5. What is the significance of Bernstein's condition to detect parallelism ?
6. Describe the cache inconsistencies caused by process migration.
7. Justify the statement : "Multiple functional units as well as Hazard avoidance improve throughput of pipelined processor".
8. Distinguish between static and dynamic interconnection network.
9. Compare multiprocessors and multicomputers.
10. Describe multithreaded architecture.

(10×4=40 Marks)

P.T.O.

PART – B

Each question carries **20** marks.

Module – I

11. a) Analyze the dependencies among the following statements in a given program. Show the dependence graphs among the statements with justification

```
DO 10 I = 1, N
    A (I + 1) = B (I – 1) + C (I)
    B (I) = A (I) * K
    C (I) = B (I) – 1
CONTINUE
```

b)

```
S1 : Load R1, M (100)        /R1 ←Memory (100)/
S2 : Move R2, R1             /R2 ←(R1)/
S3 : Inc R1                  /R1 ←(R1) + 1/
S4 : Add R2, R1              /R2 ←(R2) + (R1)/
S5 : Store M (100), R1       /Memory (100) ←(R1)/
```

Where (Ri) means the content of register Ri.

i) Draw dependence graph to show all the dependences with justification.

ii) Are there any resource dependences if only one copy of each functional unit is available in the CPU ?

OR

12. Consider the execution of the following code segment consisting of seven statements. Use Bernstein's conditions to detect the maximum parallelism embedded in this code. Justify the portions that can be executed in parallel and the remaining portions that must be executed sequentially. Rewrite the code using parallel constructs such as Cobegin and Coend. No variable substitution is allowed. All statements can be executed in parallel if they are declared within the same block of a (Cobegin, Coend) pair

```
S1 :  A = B + C
S2 :  C = D + E
S3 :  F = G + E
S4 :  C = A + F
S5 :  M = G + C
S6 :  A = L + C
S7 : A = E + A
```

Module – II

13. Consider the five-stage pipelined processor specified by the following reservation table :

	1	2	3	4	5	6
S1	X					X
S2		X			X	
S3			X			
S4				X		
S5		X				X

a) List the set of forbidden latencies and collision vector.

b) Draw state transition diagram showing all possible initial sequences (cycle) without causing a collision in the pipeline.

c) List all the simple cycles from the state diagram.

d) Identify the greedy cycles among the simple cycles.

e) What is the minimum average latency (MAL) of this pipeline ?

f) What is the minimum allowed constant cycle in using this pipeline ?

g) What will be the maximum throughput of this pipeline ?

h) What will be the throughput if the minimum constant cycle is used ?

OR

14. a) What is the use of reorder buffer ?

b) Discuss the various instruction issue and completion policies with and without instruction look ahead in a superscalar processor.

Module – III

15. a) Explain any two cache coherence protocol.

b) Describe how multiport memories used in multistage networks.

OR

16. a) Explain blocking and non-blocking network with the help of Omega network.

b) Describe data flow in hybrid architecture. **(3×20=60 Marks)**